CLAIMS:

The invention claimed is:

1. A method of forming a conductive contact to a source/drain region of a field effect transistor, comprising:

providing gate dielectric material intermediate a transistor gate and a channel region of a field effect transistor, at least some of the gate dielectric material extending to be received over at least one source/drain region of the field effect transistor; and

exposing the gate dielectric material received over the one source/drain region to conditions effective to change it from being electrically insulative to being electrically conductive and in conductive contact with the one source/drain region.

2. The method of claim 1 wherein the extending gate dielectric material has a dielectric constant of at least 8.

3. The method of claim 1 wherein the exposing forms the extending material to comprise a conductive metal nitride.

4. The method of claim 3 wherein the exposing forms the extending material to comprise an elemental metal followed by formation of the conductive metal nitride.

5. The method of claim 1 wherein the exposing forms the extending material to comprise a conductive metal boride.

6. The method of claim 5 wherein the exposing forms the extending material to comprise an elemental metal followed by formation of the conductive metal nitride.

7. The method of claim 1 wherein the exposing forms the extending material to comprise a conductive metal silicide.

8. The method of claim 7 wherein the one source/drain region comprises silicon, and the silicide is formed by reaction of metal of the extending gate dielectric material with silicon of the one source/drain region.

9. The method of claim 7 wherein the conductive metal silicide is formed by exposure to a silicon comprising atmosphere.

10. The method of claim 1 wherein the exposing forms the extending material to comprise an elemental metal.

11. The method of claim 1 wherein the exposing forms the extending material to comprise a conductive metal oxide.

12. The method of claim 1 wherein the exposing forms the extending material to comprise a conductive metal carbide.

13. The method of claim 1 wherein the exposing forms the extending material to comprise a conductive metal sulfide.

14. The method of claim 1 wherein the exposing forms the extending material to comprise a conductive metal halide.

15. The method of claim 1 wherein the extending gate dielectric material comprises a metal oxide.

16. The method of claim 15 wherein the metal oxide comprises hafnium oxide.

17. The method of claim 15 wherein the metal oxide comprises aluminum oxide.

18. The method of claim 15 wherein the metal oxide comprises tantalum oxide.

19. The method of claim 15 wherein the metal oxide comprises titanium oxide.

20. The method of claim 15 wherein the metal oxide comprises hafnium oxide.

21. The method of claim 1 wherein the extending gate dielectric material comprises a metal silicate.

22. The method of claim 1 wherein the exposing forms the extending material to be homogeneous.

23. The method of claim 1 wherein the exposing forms the extending material to not be homogeneous.

24. The method of claim 23 wherein the exposing forms the extending material to comprise a conductive metal nitride received over a conductive metal silicide.

25. The method of claim 24 wherein the one source/drain region comprises silicon, and the silicide is formed by reaction of metal of the extending gate dielectric material with silicon of the one source/drain region.

26. The method of claim 1 wherein the exposing comprises exposure to plasma.

27. The method of claim 26 wherein the extending gate dielectric comprises a metal oxide, and the plasma exposure comprises at least some exposure to a reaction-inert material which breaks metal-oxygen bonds of the metal oxide.

28. The method of claim 26 wherein the extending gate dielectric comprises a metal silicate, and the plasma exposure comprises at least some exposure to a reaction-inert material which breaks metal-oxygen bonds of the metal silicate.

29. The method of claim 26 wherein the exposing comprises:

depositing another material over the extending gate dielectric material, the another material being different in composition from that of the extending gate dielectric material, the extending gate dielectric material and the another material being proximate one another at an interface, the extending gate dielectric material and the another material as being proximate one another at the interface being capable of reacting with one another at some minimum reaction temperature when in an inert non-plasma atmosphere at a pressure;

providing the interface at a processing temperature which is at least 50°C below the minimum reaction temperature and at the pressure; and

with the interface at the processing temperature and at the pressure, exposing the substrate to a plasma effective to impart a reaction of the extending gate dielectric material with the another material to form a reaction product third material in conductive contact with the one source/drain region.

30. The method of claim 29 wherein the exposing comprises ion implantation.

31. The method of claim 1 wherein the exposing is void of exposure to plasma.

32. The method of claim 1 wherein the exposing comprises ion implantation.

33. The method of claim 1 wherein all of an elevational thickness of the gate dielectric material extends to be received over the one source/drain region.

34. The method of claim 1 wherein the field effect transistor is formed over a semiconductor substrate and is oriented generally horizontally relative to the substrate.

35. The method of claim 1 wherein the field effect transistor is formed over a semiconductor substrate and is oriented generally vertically relative to the substrate.

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36. A method of forming a conductive contact to a source/drain region of a field effect transistor, comprising:

providing gate dielectric material intermediate a transistor gate and a channel region of a field effect transistor, at least some of the gate dielectric material extending to be received over at least one source/drain region of the field effect transistor;

forming a dielectric layer over the transistor gate and the one source/drain region;

forming a contact opening into the dielectric layer to the gate dielectric material received over the one source/drain region;

after forming the contact opening, exposing the gate dielectric material received over the one source/drain region to conditions effective to change it from being electrically insulative to being electrically conductive and in conductive contact with the one source/drain region; and

providing conductive material within the contact opening in electrical connection with the one source/drain region through the changed extending material.

37. The method of claim 36 wherein the field effect transistor is formed over a semiconductor substrate and is oriented generally vertically relative to the substrate.

38. The method of claim 37 wherein the transistor gate and gate dielectric material comprises an annulus formed about the channel region, the one source/drain region comprising a semiconductive material projection extending from the channel region, the projection having top and side surfaces over which the gate dielectric material is received, the exposing occurring through the contact opening to at least a portion of the gate dielectric material received over the top surface of the one source/drain region.

39. The method of claim 36 wherein the field effect transistor is formed over a semiconductor substrate and is oriented generally horizontally relative to the substrate.

40. The method of claim 36 wherein the conductive material is different in composition from that of the changed extending material.

41. The method of claim 36 wherein the conductive material and the changed extending material comprise the same composition.

42. The method of claim 36 wherein the conductive material is provided within the contact opening after the exposing.

43. The method of claim 36 wherein the conductive material is provided within the contact opening before the exposing.

44. The method of claim 36 wherein the exposing forms the extending material to comprise a conductive metal nitride.

45. The method of claim 36 wherein the exposing forms the extending material to comprise a conductive metal boride.

46. The method of claim 36 wherein the exposing forms the extending material to comprise a conductive metal silicide.

47. The method of claim 36 wherein the exposing forms the extending material to comprise an elemental metal.

48. The method of claim 36 wherein the extending gate dielectric material comprises a metal oxide.

49. The method of claim 36 wherein the extending gate dielectric material comprises a metal silicate.

50. The method of claim 36 wherein the exposing forms the extending material to be homogeneous.

51. The method of claim 36 wherein the exposing forms the extending material to not be homogeneous.

52. The method of claim 36 wherein the exposing comprises exposure to plasma.

53. The method of claim 36 wherein the exposing comprises:

depositing another material over the extending gate dielectric material, the another material being different in composition from that of the extending gate dielectric material, the extending gate dielectric material and the another material being proximate one another at an interface, the extending gate dielectric material and the another material as being proximate one another at the interface being capable of reacting with one another at some minimum reaction temperature when in an inert non-plasma atmosphere at a pressure;

providing the interface at a processing temperature which is at least 50°C below the minimum reaction temperature and at the pressure; and

with the interface at the processing temperature and at the pressure, exposing the substrate to a plasma effective to impart a reaction of the extending gate dielectric material with the another material to form a reaction product third material in conductive contact with the one source/drain region.

54. The method of claim 36 wherein the exposing is void of exposure to plasma.

55. The method of claim 36 wherein the exposing comprises ion implantation.

56. A method of forming a local interconnect, comprising:

providing gate dielectric material intermediate a transistor gate and a channel region of a field effect transistor over a semiconductor substrate, at least some of the gate dielectric material extending to be received between first and second node regions of the semiconductor substrate; and

exposing the gate dielectric material received between the first and second node regions to conditions effective to change it from being electrically insulative to being electrically conductive and forming a local interconnect from the changed material which electrically connects the first and second node regions.

57. The method of claim 56 wherein the gate dielectric material extends to be received over at least one of the first and second node regions.

58. The method of claim 57 wherein the gate dielectric material extends to be received over both the first and second node regions.

59. The method of claim 56 wherein at least one of the first and second node regions comprises conductively doped semiconductive material.

60. The method of claim 59 wherein both of the first and second node regions comprise conductively doped semiconductive material.

61. The method of claim 56 wherein at least one of the first and second node regions comprises at least one of an elemental metal and a conductive metal compound.

62. The method of claim 61 wherein both of the first and second node regions comprise at least one of an elemental metal and a conductive metal compound.

63. The method of claim 56 wherein one of the first and second node regions comprises conductively doped semiconductive material, and the other of the first and second node regions comprises at least one of an elemental metal and a conductive metal compound.

64. The method of claim 56 wherein one of the first and second node regions comprises a source/drain region of the field effect transistor.

65. The method of claim 64 wherein the other of the first and second node regions comprises conductively doped semiconductive material.

66. The method of claim 64 wherein the other of the first and second node regions comprises at least one of an elemental metal and a conductive metal compound.

67. The method of claim 64 wherein the other of the first and second node regions comprises a source/drain region of another field effect transistor.

68. The method of claim 56 wherein an outline of the local interconnect is formed before the exposing.

69. The method of claim 68 wherein the exposing is through a patterned opening formed within a masking layer.

70. The method of claim 69 wherein the masking layer comprises photoresist.

71. The method of claim 56 wherein an outline of the local interconnect is formed after the exposing.

72. The method of claim 56 wherein the local interconnect is not in direct electrical connection with any component of the field effect transistor.

73. The method of claim 56 wherein the extending gate dielectric material has a dielectric constant of at least 8.

74. The method of claim 56 wherein the exposing forms the local interconnect to comprise a conductive metal nitride.

75. The method of claim 74 wherein the exposing forms the local interconnect to comprise an elemental metal followed by formation of the conductive metal nitride.

76. The method of claim 56 wherein the exposing forms the extending material to comprise a conductive metal boride.

77. The method of claim 56 wherein the exposing forms the local interconnect to comprise a conductive metal silicide.

78. The method of claim 77 wherein the gate dielectric material received between the first and second node regions is formed on silicon, the silicide being formed by reaction of metal of the gate dielectric material received between the first and second node regions with silicon on which the gate dielectric material is received between the first and second node regions.

79. The method of claim 77 wherein the conductive metal silicide is formed by exposure to a silicon comprising atmosphere.

80. The method of claim 56 wherein the exposing forms the local interconnect to comprise an elemental metal.

81. The method of claim 56 wherein the extending gate dielectric material comprises a metal oxide.

82. The method of claim 81 wherein the metal oxide comprises hafnium oxide.

83. The method of claim 81 wherein the metal oxide comprises aluminum oxide.

84. The method of claim 81 wherein the metal oxide comprises tantalum oxide.

85. The method of claim 81 wherein the metal oxide comprises titanium oxide.

86. The method of claim 81 wherein the metal oxide comprises zirconium oxide.

87. The method of claim 56 wherein the extending gate dielectric material comprises a metal silicate.

88. The method of claim 56 wherein the exposing forms the local interconnect to be homogeneous.

89. The method of claim 56 wherein the exposing forms the local interconnect to not be homogeneous.

90. The method of claim 89 wherein the exposing forms the local interconnect to comprise a conductive metal nitride received over a conductive metal silicide.

91. The method of claim 90 wherein the gate dielectric material received between the first and second node regions is formed on silicon, the silicide being formed by reaction of metal of the gate dielectric material received between the first and second node regions with silicon on which the gate dielectric material is received between the first and second node regions.

92. The method of claim 56 wherein the exposing comprises exposure to plasma.

93. The method of claim 92 wherein the gate dielectric material received between the first and second node regions comprises a metal oxide, and the plasma exposure comprises at least some exposure to a reaction-inert material which breaks metal-oxygen bonds of the metal oxide.

94. The method of claim 92 wherein the gate dielectric material received between the first and second node regions comprises a metal silicate, and the plasma exposure comprises at least some exposure to a reaction-inert material which breaks metal-oxygen bonds of the metal silicate.

95. The method of claim 92 wherein the exposing comprises:

depositing another material over the gate dielectric material received between the first and second node regions, the another material being different in composition from that of the gate dielectric material received between the first and second node regions, the gate dielectric material received between the first and second node regions and the another material being proximate one another at an interface, the gate dielectric material received between the first and second node regions and the another material as being proximate one another at the interface being capable of reacting with one another at some minimum reaction temperature when in an inert non-plasma atmosphere at a pressure;

providing the interface at a processing temperature which is at least 50°C below the minimum reaction temperature and at the pressure; and

with the interface at the processing temperature and at the pressure, exposing the substrate to a plasma effective to impart a reaction of the gate dielectric material received between the first and second node regions with the another material to form the local interconnect to comprise a reaction product third material.

96. The method of claim 95 wherein the exposing comprises ion implantation.

97. The method of claim 56 wherein the exposing is void of exposure to plasma.

98. The method of claim 56 wherein the exposing comprises ion implantation.

99. A method of forming a local interconnect, comprising:

providing capacitor dielectric material proximate a first capacitor electrode over a semiconductor substrate, at least some of the capacitor dielectric material extending to be received between first and second node regions of the semiconductor substrate; and

exposing the capacitor dielectric material received between the first and second node regions to conditions effective to change it from being electrically insulative to being electrically conductive and forming a local interconnect from the changed material which electrically connects the first and second node regions.

100. The method of claim 99 wherein the capacitor dielectric material extends to be received over at least one of the first and second node regions.

101. The method of claim 100 wherein the capacitor dielectric material extends to be received over both the first and second node regions.

102. The method of claim 99 comprising forming a second capacitor electrode of a capacitor comprising the first capacitor electrode, the second capacitor electrode and the capacitor dielectric material received between the first and second capacitor electrodes; the second capacitor electrode being formed prior to the exposing.

103. The method of claim 99 comprising forming a second capacitor electrode of a capacitor comprising the first capacitor electrode, the second capacitor electrode and the capacitor dielectric material received between the first and second capacitor electrodes; the second capacitor electrode being formed after the exposing.

104. The method of claim 99 wherein at least one of the first and second node regions comprises conductively doped semiconductive material.

105. The method of claim 104 wherein both of the first and second node regions comprise conductively doped semiconductive material.

106. The method of claim 99 wherein at least one of the first and second node regions comprises at least one of an elemental metal and a conductive metal compound.

107. The method of claim 106 wherein both of the first and second node regions comprise at least one of an elemental metal and a conductive metal compound.

108. The method of claim 99 wherein one of the first and second node regions comprises conductively doped semiconductive material, and the other of the first and second node regions comprises at least one of an elemental metal and a conductive metal compound.

109. The method of claim 99 wherein an outline of the local interconnect is formed before the exposing.

110. The method of claim 109 wherein the exposing is through a patterned opening formed within a masking layer.

111. The method of claim 110 wherein the masking layer comprises photoresist.

112. The method of claim 99 wherein an outline of the local interconnect is formed after the exposing.

113. The method of claim 99 wherein the extending capacitor dielectric material has a dielectric constant of at least 8.

114. The method of claim 99 wherein the exposing forms the local interconnect to comprise a conductive metal nitride.

115. The method of claim 114 wherein the exposing forms the local interconnect to comprise an elemental metal followed by formation of the conductive metal nitride.

116. The method of claim 99 wherein the exposing forms the extending material to comprise a conductive metal boride.

117. The method of claim 99 wherein the exposing forms the local interconnect to comprise a conductive metal silicide.

118. The method of claim 117 wherein the capacitor dielectric material received between the first and second node regions is formed on silicon, the silicide being formed by reaction of metal of the capacitor dielectric material received between the first and second node regions with silicon on which the capacitor dielectric material is received between the first and second node regions.

119. The method of claim 117 wherein the conductive metal silicide is formed by exposure to a silicon comprising atmosphere.

120. The method of claim 99 wherein the exposing forms the local interconnect to comprise an elemental metal.

121. The method of claim 99 wherein the extending capacitor dielectric material comprises a metal oxide.

122. The method of claim 121 wherein the metal oxide comprises hafnium oxide.

123. The method of claim 121 wherein the metal oxide comprises aluminum oxide.

124. The method of claim 121 wherein the metal oxide comprises tantalum oxide.

125. The method of claim 121 wherein the metal oxide comprises titanium oxide.

126. The method of claim 121 wherein the metal oxide comprises zirconium oxide.

127. The method of claim 99 wherein the extending capacitor dielectric material comprises a metal silicate.

128. The method of claim 99 wherein the exposing forms the local interconnect to be homogeneous.

129. The method of claim 99 wherein the exposing forms the local interconnect to not be homogeneous.

130. The method of claim 129 wherein the exposing forms the local interconnect to comprise a conductive metal nitride received over a conductive metal silicide.

131. The method of claim 130 wherein the capacitor dielectric material received between the first and second node regions is formed on silicon, the silicide being formed by reaction of metal of the capacitor dielectric material received between the first and second node regions with silicon on which the capacitor dielectric material is received between the first and second node regions.

132. The method of claim 99 wherein the exposing comprises exposure to plasma.

133. The method of claim 132 wherein the capacitor dielectric material received between the first and second node regions comprises a metal oxide, and the plasma exposure comprises at least some exposure to a reaction-inert material which breaks metal-oxygen bonds of the metal oxide.

134. The method of claim 132 wherein the capacitor dielectric material received between the first and second node regions comprises a metal silicate, and the plasma exposure comprises at least some exposure to a reaction-inert material which breaks metal-oxygen bonds of the metal silicate.

135. The method of claim 132 wherein the exposing comprises:

depositing another material over the capacitor dielectric material received between the first and second node regions, the another material being different in composition from that of the capacitor dielectric material received between the first and second node regions, the capacitor dielectric material received between the first and second node regions and the another material being proximate one another at an interface, the capacitor dielectric material received between the first and second node regions and the another material as being proximate one another at the interface being capable of reacting with one another at some minimum reaction temperature when in an inert non-plasma atmosphere at a pressure;

providing the interface at a processing temperature which is at least 50°C below the minimum reaction temperature and at the pressure; and

with the interface at the processing temperature and at the pressure, exposing the substrate to a plasma effective to impart a reaction of the capacitor dielectric material received between the first and second node regions with the another material to form the local interconnect to comprise a reaction product third material.

136. The method of claim 135 wherein the exposing comprises ion implantation.

137. The method of claim 99 wherein the exposing is void of exposure to plasma.

138. The method of claim 99 wherein the exposing comprises ion implantation.